

Description

Semiconductor device with plastic package molding compound, semiconductor chip and leadframe and method
5 for producing the same

The invention relates to a semiconductor device with a plastic package molding compound, a semiconductor chip and a leadframe and to a method for producing the same.
10 The semiconductor chip is embedded with one of its upper sides and its peripheral sides in the plastic package molding compound. The other upper side of the semiconductor chip is arranged on the leadframe. The upper side of the leadframe that is not covered by the
15 semiconductor chip is covered by the plastic package molding compound.

Such a construction of a semiconductor device is held together by the fixing plastic package molding
20 compound, which at the same time embeds the semiconductor chip and is firmly anchored on the leadframe. The semiconductor chip is additionally fixed in its position on the leadframe by means of an adhesive layer, the adhesive layer ensuring that the
25 semiconductor chip is neither displaced during the application of the plastic package molding compound nor lifts off from the leadframe. At the same time, the adhesive layer under the semiconductor chip acts as a stress equalizing layer when thermal stresses occur.

30 However, the actual equalizing effect of the adhesive layer under the semiconductor chip is not fully realized, since it is enclosed on all sides by the rigid plastic package molding compound. Consequently,
35 the adhesive layer, which is restricted to the surface of the semiconductor chip, is also laterally fixed and cannot completely equalize the difference in stress between the leadframe and the semiconductor chip that

is caused by the different coefficients of expansion. Consequently, in temperature cycle tests virtually the entire stress between the semiconductor chip and the circuit substrate is passed on to the external contacts
5 of the semiconductor device, which can lead to considerable failures.

In spite of the equalization of thermal stresses by the adhesive layer between the semiconductor chip and the
10 leadframe, microcracks can also occur in the case of such a construction of a semiconductor device, in particular at the boundary layer between the plastic package molding compound and the upper sides of the leadframe. It has previously been attempted to prevent
15 such microcracks, which in an extreme case can lead to delamination, by strengthening the anchorages between the two materials. For this purpose, porous ceramic or metallic coatings have been developed for the upper side of the leadframe and deposited on the leadframe in
20 order to improve the anchorage with the plastic package molding compound. Nevertheless, it is observed that the stronger anchorage has the effect that the formation of microcracks is shifted into regions above the anchoring layer but cannot be completely
25 suppressed.

The object of the invention is to provide a semiconductor device with a plastic package molding compound, a semiconductor chip and a leadframe that
30 solves the problems of current semiconductor devices in the transitional region from the leadframe to the plastic package molding compound and at the transition to the semiconductor chip material and makes an improved yield possible after a temperature cycle test.

35 The above object is achieved by the subject matter of the independent claims. Advantageous developments of the invention are provided by the dependent claims.

The invention provides a semiconductor device with a plastic package molding compound, a semiconductor chip and a leadframe in which the semiconductor chip is embedded with one of its upper sides and its peripheral sides in the plastic package molding compound. The other of the two upper sides is surface-mounted on an upper side of the leadframe. The region of the upper side of the leadframe that is not covered by the semiconductor chip is covered by the plastic package molding compound. Arranged between the plastic package molding compound and the leadframe, and between the semiconductor chip and the leadframe, on the upper side of the leadframe is a continuous, elastic adhesive layer.

Consequently, in the case of the semiconductor device according to the invention, intensive anchorage of the plastic package molding compound with the embedded semiconductor chip on the leadframe is not an objective, but rather the two regions are decoupled by the continuous elastic adhesive layer arranged between them. With devices of a conventional type, it has been found in temperature cycle tests that the boundary layer between these regions of the plastic package molding compound with the semiconductor chip and of the leadframe, which expand differently, are subjected to extreme loading and have the tendency for microcracks to form, which is overcome by the device according to the invention. In an extreme case, these microcracks lead to delamination, but not in the case of the device according to the invention. Conventional devices at least provide conducive conditions for the penetration of moisture into the microcracks at high temperature, the moisture which has penetrated then being capable of rupturing the device at the extreme cooling temperatures of the temperature cycle test, which in

the case of the device according to the invention is prevented by the adhesive layer.

5 The advantage of the semiconductor device according to the invention is that, by contrast with the tendency to strengthen the anchorage between the different materials and constantly improve the mechanical coupling and increase the rigidity of the device, in the case of the semiconductor device according to the
10 invention the anchorage or the coupling of the upper side of the leadframe to the plastic package molding compound is relaxed, or eliminated completely, by a rubber-elastic adhesive layer.

15 Consequently, in the case of the semiconductor device according to the invention, a decoupling of the expansion behavior of the components on the upper side of the leadframe from the material of the leadframe is created, which leads to the formation of microcracks
20 being reduced and the risk of delamination being avoided. It is of particular advantage if an elastomer-based adhesive layer is arranged on the upper side of the leadframe, since such elastomers can tolerate a great difference in the expansion behavior
25 of the materials without microcracks forming or delamination occurring. Adhesive gel is also a means that can be successfully used to realize such an adhesive layer. Silicone-based elastomers are extremely significant in this respect.

30 In one embodiment of the invention it is provided that the peripheral regions of the semiconductor device are free of the elastic adhesive layer. This region that is free of the elastic adhesive layer is minimized as
35 far as possible in its area requirement and surrounds the entire periphery of the device.

This embodiment of the invention is accompanied by the advantage that the adhesive compound of the adhesive layer does not lead to soiling of the dividing tools during the singulating of semiconductor devices from a panel. This is especially since adhesive compounds on the dividing tools can lead to considerable problems in fabrication, which is not permissible when they are used in mass production. Consequently, keeping the peripheral regions of the semiconductor device free of the elastic adhesive layer has a not inconsiderable advantage for fabrication. However, keeping them free in this way can have the effect that, in the peripheral regions, microcracks then occur to an increased extent in the plastic package molding compound, which then rests in the peripheral regions on the leadframe without a decoupling elastic adhesive layer.

A further embodiment of the invention provides that the peripheral regions of the semiconductor device kept free of the adhesive layer have elastic metal layers. Such metal layers may be made to match one another in such a way that a stress reduction takes place in them, without leading to the formation of microcracks. For this purpose, a copper layer which comprises a copper alloy may be arranged on the leadframe, and a gold layer of a gold alloy may be deposited on top of it in the peripheral region, elastic deformations of the soft metals serving to reduce stresses without microcrack formations occurring. Furthermore, the anchorage of the plastic package molding compound on the gold coating is minimal, so that, apart from a ductile displacement, a deliberate microgap formation can occur, which however then does not cause any microcracks in the plastic package molding compound.

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Instead of a gold layer, silver or aluminum layers may also be deposited on the copper layer, since these metals also comprise alloys which are extremely ductile

and can consequently yield in a ductile manner under stress loading without microcracks forming. For this purpose, the width of the metal layers in the peripheral regions of the semiconductor device may be adapted to the width of sawing tracks in such a way that the elastic adhesive layer is not exposed to the sawing process in the production of the peripheral sides of the semiconductor device. For this purpose, the ratio between the width of the metal layer and the width of the sawing tracks preferably lies between 1.2 and 3. In this respect, allowance is made for the adjustment tolerance in the alignment for the sawing process and the sawing tolerance, in order to determine the ratio between the width of the metal layers and the width of the sawing tracks more precisely.

A further aspect of the invention relates to a panel which has device positions with semiconductor devices arranged in rows and columns, as described above. Such a panel is in practice a composite sheet comprising the plastic package molding compound, the semiconductor chips and the leadframe which has semiconductor devices arranged in a number of device positions. Such a panel may take the form of a rectangular sheet or be modelled on a semiconductor wafer, so that customary automatic dividing machines can be used for dividing the wafer.

A method for producing such a panel with a plastic package molding compound, semiconductor chips and a leadframe in a number of semiconductor device positions has the following method steps. Firstly, a leadframe with device positions arranged in rows and/or columns is produced. Such a leadframe may comprise a sheet of insulating plastic which has on the underside of the leadframe a wiring structure, which for its part has wiring leads and external contact areas.

The wiring leads in this case lead to bonding fingers, which are arranged at the periphery of a central opening in the leadframe. The central opening makes access possible to contact areas of a semiconductor device which is aligned on the basis of this opening. However, even before such a semiconductor chip is applied to the opening, an elastic adhesive layer, covering both the region of the intended semiconductor chip and the region of the intended plastic package molding compound on an upper side of the leadframe in the device positions. Subsequently, semiconductor chips are aligned with the adhesive layer in the device positions and adhesively attached.

In the event that the circuit substrate has a central opening, it is ensured when adhesively attaching the semiconductor chip that contact areas of the axial upper side of the semiconductor chip which are arranged in bonding channels are aligned in a way corresponding to the opening in the leadframe in the device positions.

Subsequently, electrical connections are established between contact areas of the semiconductor chip and the leadframe in the device positions. In the case of a central bonding channel, the contact areas, which are arranged for example in two rows in the central bonding channel, may be connected to the bonding fingers of the wiring structure on the underside of the leadframe by means of bonding wires. Subsequently, the plastic package molding compound is applied to the adhesive layer while embedding the semiconductor chips and while forming a panel with a number of semiconductor device positions. In the case of a bonding channel opening on the rear side of the leadframe, this may also be sealed when a plastic package molding compound is applied.

This method has the advantage that individual method steps can be carried out simultaneously in parallel for a number of semiconductor device positions. In addition, the method has the advantage that it can be
5 used to create a panel of which the upper region, that is the region of the plastic package molding compound and the semiconductor chips, is decoupled from its lower region, the leadframe with bonding connections, in the respective expansion behavior.

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For the production of a semiconductor device, it is merely necessary to divide the panel up into individual semiconductor devices along the dividing tracks or sawing tracks, the semiconductor devices still not
15 having external contacts. The external contacts may be applied both before the dividing up of the panel and after the dividing up of the panel to the respective external contact areas of the wiring structure on the underside of the leadframe.

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If the external contacts are applied before the dividing up of the panel, this has the advantage that the external contacts can also be applied to the external contact areas and connected to the external
25 contact areas simultaneously for a number of semiconductor devices in one method step. In the case of a method in which it envisaged only to divide the devices in each device position and subsequently apply external contacts to external contact areas, the
30 advantage is obtained that external contacts are to be applied only to the semiconductor devices which have previously not been marked as defective devices during the functional test of the panel.

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In a further example of how the method is carried out, it is provided that a pattern of metal layers is applied to the leadframe before the application of the adhesive layer. This pattern covers on the one hand

the sawing tracks with the metal layers and on the other hand the peripheral regions of each device position. In this case, the width of the metal layers is in a ratio to the width of the sawing tracks of
5 between approximately 1.2 and 3. This ratio can be adapted precisely to the tolerances of the sawing track widths and the tolerances of the means allowing alignment of the panel in the preparation for sawing. If the tolerances are relatively narrow, it is possible
10 to go back to the minimum width of 1.2 in the ratio to the sawing track width, and if the tolerances are correspondingly high, widths of up to three times the sawing track width may be provided.

15 These metal layers on the one hand have the advantage that they can follow the thermal expansions of the components of the semiconductor device and thereby change in a ductile manner without forming microcracks or initiating microgaps in a desired peripheral region.
20 Furthermore, the application of the metal layers has the advantage that sawing tools are not soiled by the rubber-elastic material of the adhesive layer, and consequently last through longer servicing intervals, which considerably brings down fabrication costs.

25 To sum up, it can be stated that the basic idea of the invention of extending the adhesive layer to the periphery of the package, or at most taking it up to the singulation tolerance of a sawing track, is
30 accompanied by the advantage that the elastic adhesive layer, which reduces thermal stresses, is no longer restricted in its expansion behavior by the plastic package molding compound. If, for example, a layer of gold is additionally introduced into the boundary layer
35 in the peripheral regions of the semiconductor device, the region of the plastic package molding compound with the semiconductor chip is likewise mechanically decoupled from the leadframe. This is especially since

a layer of gold has lower adhesion in relation to the plastic package molding compound than the otherwise customary solder resist masks or anchorage coatings of conventional devices.

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Consequently, a complete path for decoupling between the semiconductor chip and in the plastic package molding compound the leadframe can be achieved by the following measures according to the invention:

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1. The geometry of the adhesive layer is designed in such a way that a defined mold periphery remains, which ensures formation of a gap between the metal layers and the plastic package molding compound, the adhesive layer being taken up to the periphery of the package as far as the singulation tolerance.

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2. A gold periphery is placed on the upper side of the leadframe in the peripheral region, applied to a copper layer or to a solder layer which are present in any case in the production of the leadframe. Since the plastic package molding compound adheres poorly on the gold, local points of reduced adhesion are obtained, and consequently a desired gap between the layer of gold and the plastic package molding compound.

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Consequently, the semiconductor chip with the plastic package molding compound is decoupled virtually completely from the leadframe by this invention, the different expansions on account of different coefficients of expansion being compensated by the adhesive layer. In addition, in the case in which the adhesive does not extend completely up to the periphery of the semiconductor device, the singulation process, i.e. the sawing technique, is not impaired.

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The gap possibly forming in the boundary surface between the gold layer and the plastic package molding compound may serve at the same time as a moisture path, so that the mechanical decoupling advantageously results at the same time in the formation of a deliberately arranged moisture path for the moisture test.

To sum up, the following advantages of the invention can be stated:

1. The extended adhesive layer, or adhesive layer of increased surface area, mechanically decouples the semiconductor chip from the circuit substrate and thereby equalizes the different coefficients of expansion.
2. Deliberate gap formation allows the creation of a decoupling path, which is based on intentional worsening of the adhesion between the metal layers and the plastic package molding compound.
3. In the case of the semiconductor device according to the invention, an increased thermal cycling endurance is found.
4. Advantageous path formation for the moisture test is achieved.
5. Greater reliability for the semiconductor devices can be ensured.

The invention is now explained in more detail on the basis of the accompanying figures.

Figure 1 shows a schematic cross section through a semiconductor device of a first embodiment of the invention.

Figure 2 shows a schematic cross section through a semiconductor device of a second embodiment of the invention.

Figure 1 shows a schematic cross section through a semiconductor device 1 of a first embodiment of the invention. The semiconductor device 1 comprises two regions, which are held together by means of an elastic adhesive layer 11. The upper region of the semiconductor device 1 is arranged on the adhesive layer 11 and has a semiconductor chip 3, which is fixed on the adhesive layer 11 by its active upper side 7. Also arranged on the adhesive layer 11 is a plastic package molding compound 2, which embeds the peripheral sides 5 and 6 of the semiconductor chip 3 and the rear side 8 of the semiconductor chip 3. The adhesive layer 11 may be made up of a single layer of adhesive of a rubber-elastic material, or comprise a film which is coated with adhesive on both sides. The layer of adhesive may also be favorably printed or dispensed.

A film with layers of adhesive on both sides as the adhesive layer 11 has the advantage that it has fabrication advantages for the production of the exemplary embodiment shown in Figure 1, since it can be reproducibly positioned on the leadframe 4 in such a way that an opening 18 in the leadframe 4 remains free. The second region of the semiconductor device 1 is formed in a leadframe 4, which bears the adhesive layer 11 on its upper side 9. On its rear side 25, the leadframe 4 has a wiring structure 24, which is partially covered by a layer of solder resist 28. The wiring structure 24 has wiring leads 29, external contact areas 27 and bonding fingers 23.

The bonding fingers 23 are arranged in the peripheral region of the central opening 18 on the rear side 25 of the leadframe 4, while the external contact areas 27, which are connected to the bonding fingers 23 by means of wiring leads 29, bear external contacts 26. The lower region with the leadframe 4 and the upper region

with the semiconductor chip 3 in the plastic package molding compound 2 are electrically connected to each other by means of electrical connections 16. The electrical connections 16 have bonding wires 22, which
5 are arranged in a bonding channel 19. These bonding wires 22 connect the rows of contact areas 20 and 21 on the active upper side 7 of the semiconductor chip 3 to the bonding fingers 23 on the rear side 25 of the leadframe 4.

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The advantages of a continuous adhesive layer 11 for keeping such a device 1 together have been explained in detail above and, to avoid repetition, are not separately discussed at this point. Not only is the
15 semiconductor chip 3 embedded in the plastic package molding compound 2, but also the bonding wires 22 are embedded in such a plastic molding compound by sealing the bonding channel 19 with the plastic package molding compound 2. No explanation of the method for producing
20 such a semiconductor device 1 is given at this point either, especially since it has already been described above.

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Figure 2 shows a schematic cross section through a semiconductor device of a second embodiment of the invention. Components with the same functions as in Figure 1 are identified by the same designations and not separately explained.

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The second embodiment of the invention according to Figure 2 differs from the first embodiment of the invention according to Figure 1 in that, instead of an adhesive layer 11, a metal layer 13 is arranged between the upper part of the semiconductor device 10 and the
35 lower region of the semiconductor device 10 in the peripheral regions 12 of the semiconductor device 10. In this embodiment of the invention, this metal layer 13 comprises two components, that is a copper layer 14

on the leadframe 4 and a gold layer 15 applied on top of it.

5 The width b of the metal layer 13 is dimensioned in such a way that it is possible for a number of semiconductor devices 10 to be reliably divided from a panel along sawing tracks without an adhesive layer 11 being able to soil the dividing tool. The gold coating ensures that the adhesion of the plastic package molding compound 2 is reduced in the boundary layer between the material of the plastic package molding compound 2 and the gold coating, so that, in addition to the purely ductile compliance of the gold and copper layers 14, 15 of the metal layer 13, under extreme loading microgaps can also form in the boundary layer, on the one hand permitting a moisture path via which moisture can escape from the semiconductor device 10, whereby the moisture test is improved, and on the other hand permitting compliance in the peripheral region, whereby improved reliability in thermal cycling tests is achieved.